Toward Understanding Positive Bias Temperature Instability in Fully Recessed-Gate GaN MISFETs

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***Abstract*— In this paper, fully recessed-gate GaN MISFETs with two different gate dielectrics, i.e., plasma-enhanced atomic layer deposition (PEALD) SiN and ALD Al_2O_3 gate dielectric, are used to study the origin of positive bias temperature instability (PBTI). By employing a set of dedicated stress-recovery tests, we study PBTI during the stress and relaxation. Hence, a defect band model with different distributions of defect levels inside the gate dielectric is proposed, which can excellently reproduce the experimental data and provide insightful information about the origin of PBTI in GaN MISFETs. The results indicate that the serious PBTI in the device with PEALD SiN is mainly due to a wide distribution of defect levels ($\sigma \sim 0.67$ eV), centered below the conduction band of GaN ($E_C - 0.05$ eV), and can be easily accessed by the channel carriers already at a low-gate voltage. On the other hand, ALD Al_2O_3 gate dielectric shows a narrower distribution of defects ($\sigma \sim 0.42$ eV), which are far from the conduction band of GaN ($E_C + 1.15$ eV). This observations explain the improved PBTI reliability observed in devices with ALD Al_2O_3.**

***Index Terms*— GaN-on-Si, MISFETs, positive bias temperature instability (PBTI), recessed gate, V_{TH} hysteresis.**

I. Introduction

AlGaN/GaN-BASED power transistors have been considered as a potential candidate for power switching applications. Conventional AlGaN/GaN Schottky high-electron mobility transistors (HEMTs) suffer from high-gate leakage, resulting in an unfavorable power loss during an OFF-state condition and a low-gate overdrive during an ON-state condition. In order to tackle this issue, MIS-HEMTs have recently received significant attention for both the depletion-mode (d-mode) and enhancement-mode (e-mode) applications [1]–[6].

Inserting a dielectric at the interface between the AlGaN barrier and the gate metal significantly reduces the gate leakage current, enabling the use of a high-gate-voltage overdrive to have a fast switch from OFF-state to ON-state operation.

Up to date, threshold voltage (V_{TH}) hysteresis after a positive forward–reverse gate sweep or V_{TH} shift during a positive-gate bias stress, which is generally known as positive bias temperature instability (PBTI), has been reported for different gate dielectrics [6]–[12]. Most of the reports focus on the PBTI in the d-mode MIS-HEMTs [7]–[11], i.e., with no gate recess of the AlGaN barrier. In a cascode circuit topology, which comprises a d-mode MIS-HEMT in series with an e-mode Si MOSFET, the gate voltage will not exceed $V_G = 0$ V in the d-mode MIS-HEMT. Therefore, PBTI is not expected to be a show-stopper for d-mode MIS-HEMTs. On the contrary, both the time-dependent dielectric breakdown and the PBTI represent serious reliability issues in fully recessed-gate MISFETs for the e-mode applications, since a high-gate overdrive ($V_G - V_{TH}$) is needed for fast switching [6], [13]. So far, there is a limited literature of the PBTI in fully recessed-gate MISFETs [12]. In order to develop technologically relevant solutions, it is necessary to gain in-depth understanding of the PBTI in fully recessed-gate MISFETs.

In a previous work, we have demonstrated an extended measure-stress-measure (eMSM) technique to evaluate PBTI in fully recessed-gate GaN MISFETs [14]. In this paper, we present a comprehensive study of the PBTI in fully recessed-gate MISFETs with two different gate dielectrics plasma-enhanced atomic layer deposition (PEALD) SiN and ALD Al_2O_3, including the time exponent n measured with different dielectrics, overdrive voltage–acceleration exponent γ, mean activation energy for the charge capture and emission processes, BTI relaxation behavior, and defect-band model of charge trapping in distributed gate dielectric defect levels. First of all, the standard I_D–V_G sweep is used for the evaluation of V_{TH} hysteresis, and the standard frequency-conductance measurement is used to characterize the interface state density (D_{it}). Subsequently, a set of dedicated stress-recovery tests was used to investigate the kinetics of PBTI from different points of view. Finally, a physical model based on a gate dielectric defect band is proposed to explain the PBTI mechanisms and calibrated on the experimental data.

II. Device Fabrication

A schematic of GaN MISFETs is shown in Fig. 1. All devices were fabricated with an Au-free CMOS-compatible process on 200-mm (111) Si wafers, starting with an

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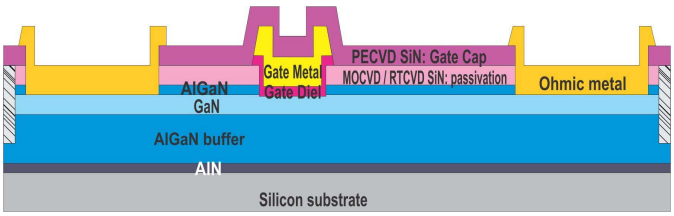


Fig. 1. Schematic of fully recessed-gate GaN MISFETs.

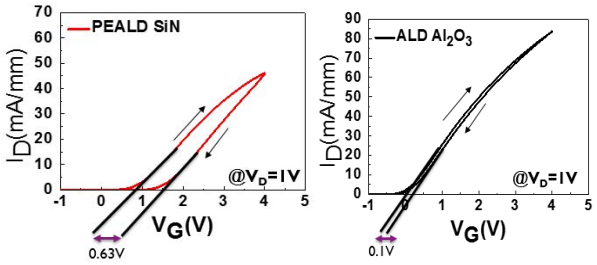


Fig. 2. I_D–V_G characteristics of the devices with (a) PEALD SiN and (b) ALD Al_2O_3 gate dielectrics. The V_{TH} hysteresis is 0.63 and 0.1 V, respectively.

AlN nucleation layer, a 2.3-μm AlGaN buffer, a 300-nm GaN channel, a 15-nm $Al_{0.25}Ga_{0.75}N$ barrier, and a 5-nm metal–organic chemical vapor deposition *in situ* SiN cap layer. Then, 140-nm rapid thermal chemical vapor deposition SiN was deposited at 750 °C. The device isolation was formed by nitrogen implantation. The SiN layer can be removed by using selectively etched SF_6-based chemistry. The recessed gate is performed by the atomic layer etch (ALE) process [15], which has no selectivity between the AlGaN and GaN layers. The 1.1-nm etching depth per cycle can be precisely controlled by an ALE process. The 17 cycles of ALE process result in 3.7-nm depth into the GaN channel. Two different gate dielectrics [PEALD SiN (20 nm) and ALD Al_2O_3 (25 nm)] were separately deposited in this paper. The PEALD (20 nm) was deposited at 300 °C and Al_2O_3 (25 nm) was deposited, followed by forming gas annealing for 1 min at 650 °C. The CMOS-compatible gate metal stack consisting of TiN/Ti/Al/Ti/TiN was deposited. Then, 200-nm PECVD SiN was deposited as a capping layer that protects the gate metal during subsequent ohmic metal process. Afterward, the ohmic metal was formed by recessing to the GaN channel and deposition of 5-nm Ti/100-nm AlCu/20-nm Ti/60-nm TiN, followed by rapid thermal anneal at 565 °C for 90 s.

III. Results and Discussion

A. I_D–V_G Characteristics and Interface Characterization

The devices were first electrically tested by a positive forward–reverse gate I_D–V_G sweep [sweeping rate: 1.5 (V/s)]. Fig. 2 shows the typical I_D–V_G characteristics after a positive forward–reverse gate sweep. The V_{TH} hysteresis is 0.63 and 0.1 V in the devices with SiN and Al_2O_3 gate dielectrics, respectively. The Al_2O_3 gate dielectric shows a smaller V_{TH} shift compared with SiN gate dielectric. The V_{TH} values are 0.7 and 0.1 V, as calculated by the criterion of $I_D = 1$ mA/mm, respectively.

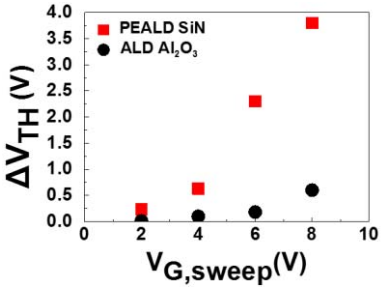


Fig. 3. Summary of ΔV_{TH} versus $V_{G,sweep}$.

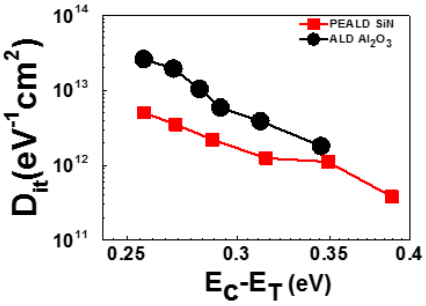


Fig. 4. D_{it} measurement in fully recessed-gate MISFETs. The trap state energy was estimated based on the Shockley–Read–Hall statistical model with an assumed capture cross section of 1×10^{-15} cm^2.

Fig. 3 shows the V_{TH} hysteresis with respect to the different gate sweep voltages.

Similar to the literature [16]–[21], a standard frequency-dependent conductance analysis was performed first as the starting point to evaluate the gate-stack quality when using these two dielectrics. Fig. 4 shows the extracted D_{it} (interface state density) values by frequency-dependent conductance method at the interface under the gate dielectric, which are $D_{it} \sim 5 \times 10^{12} - 4 \times 10^{11}$ $cm^{-2}eV^{-1}$ (PEALD SiN) and $D_{it} \sim 2 \times 10^{13} - 2 \times 10^{12}$ $cm^{-2}eV^{-1}$ (ALD Al_2O_3), respectively. The values of D_{it} are measured under the depletion region in the C–V measurements, where the gate bias is $-0.3 \sim 0.5$ V for ALD Al_2O_3 and $0.5 \sim 1$ V for PEALD SiN, respectively. However, the impact of border traps on the extracted D_{it} values cannot be excluded [11]. Therefore, a more general analysis with a set of stress-recovery tests was used to understand the PBTI, as shown in the following Section (III.B).

B. Insight Into PBTI Mechanisms

1) Extended Measure-Stress-Measure Technique: In order to further understand the PBTI mechanism, a set of stress-recovery tests was conducted. A dedicated eMSM sequence [22] was performed. This measurement technique can capture several features of the PBTI kinetics during both stress and recovery phases during a single experiment with a minimum sense delay of 1 ms. In order to avoid prestressing the device during the initial I_D–V_G characterization sweep, the I_D–V_G was only measured up to V_{TH} of the fresh device. The value of ΔV_{TH} (threshold voltage shift) was estimated from the drain current degradation, as shown in Fig. 5.

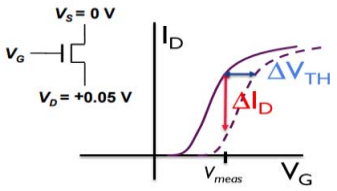


Fig. 5. ΔV_{TH} voltage is converted from the drain current reduction.

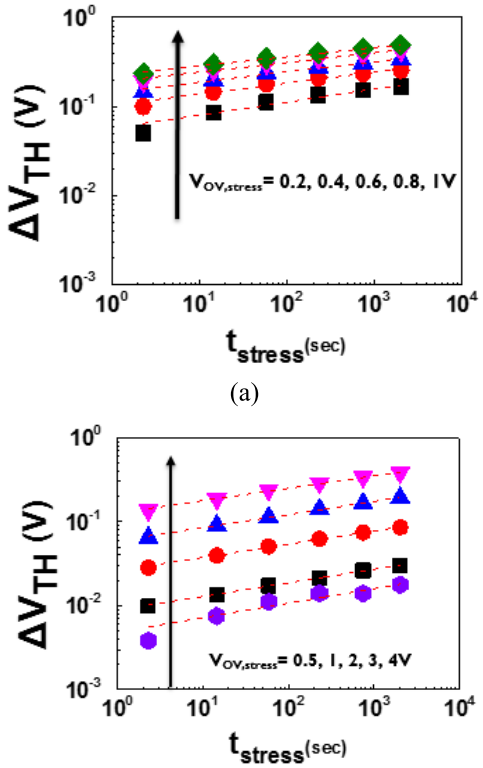


Fig. 6. ΔV_{TH} versus t_{stress} on the device with (a) PEALD SiN and (b) ALD Al_2O_3 in a logarithmic–logarithmic scale. Dashed lines: power law fits to the data [see (1)].

2) Experimental Results and Discussion: A nonlinear (i.e., a power law) dependence of ΔV_{TH} on t_{stress} was observed, as shown in Fig. 6. Large $\Delta V_{TH} > 0.1$ V was observed already at short stress time (2 s) and moderate gate stress voltages ($V_{ov,stress} = 0.4$ V) [Fig. 6(a)] in the device with PEALD SiN gate dielectric. Similar to BTI evolution in different device technologies [24], [25], [27], [29], ΔV_{TH} was also observed to follow a power law of the stress time and stress overdrive voltage:

$$\Delta V_{TH} = A_0 (V_G - V_{TH0})^{\gamma} t_{stress}^{n} \quad (1)$$

where A is the prefactor and n is the time exponent.

The time-dependence exponent n is estimated by fitting the power law (1) to each experimental curve. Fig. 7 shows the time exponent n versus $V_{OV,stress}$, where $V_{OV,stress}$ represents the difference between the gate stress voltage and the threshold voltage ($V_G - V_{TH}$). In general, the time exponent n is in the range of 0.1–0.225, which are within the typical range

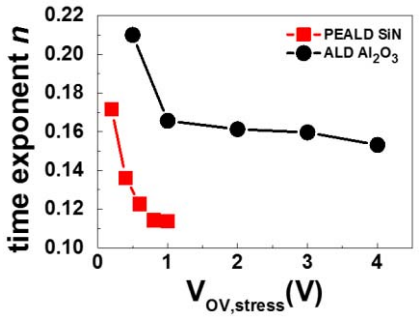


Fig. 7. Time exponent n with respect to the two different gate dielectrics.

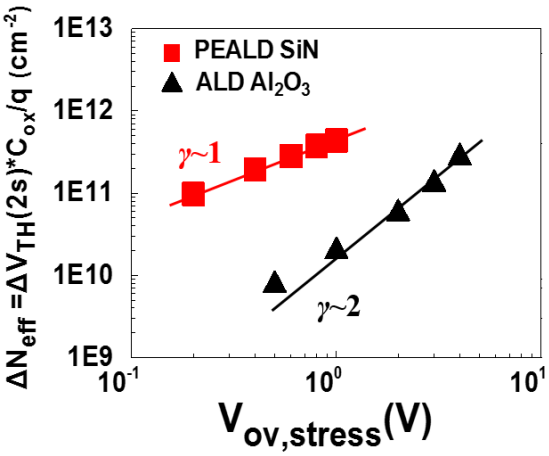


Fig. 8. PBTI shift benchmarking in terms of voltage dependence of ΔV_{TH}.

of BTI reports in different technologies [24], [25], [27], [29]. However, it is worth noting that the time exponent n of PEALD SiN decreases faster when increasing gate voltage. The smaller exponent n, i.e., the weaker stress time dependence of the ΔV_{TH} evolution, indicates that a fast ΔV_{TH} has happened very quickly as soon as the stress voltage has been applied. On the other hand, in the device with ALD Al_2O_3, we can see that the time exponent n shows a slower decreases toward higher $V_{OV,stress}$.

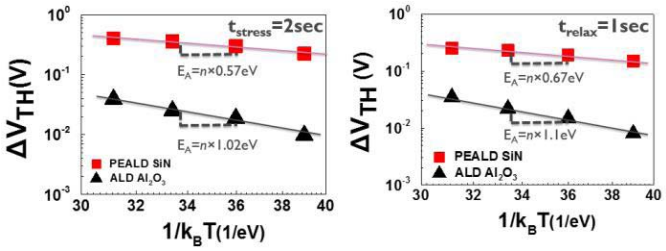
Furthermore, by extracting ΔV_{TH} after a 2-s stress, the relationship of ΔV_{TH} and $V_{OV,stress}$ can be benchmarked, as shown in Fig. 8. As one can clearly see, Al_2O_3 devices show a ~10× lower ΔV_{TH} value as compared with SiN. Moreover, a weak voltage dependence exponent $\gamma \sim 1$ is observed for PEALD SiN, while $\gamma \sim 2$ for the ALD Al_2O_3. We note that γ describes the voltage dependence of ΔV_{TH}, as shown in the following equation:

$$\Delta V_{TH} \propto V_{ov,stress}^{\gamma}. \quad (2)$$

The physical origin of different γ values will be discussed in the following Section (IV).

The ΔV_{TH} value during the stress can be expressed by using a semiempirical model [29]

$$\Delta V_{TH} \approx A_0 \exp\left(-\frac{E_A}{k_B T}\right)\left(\frac{|V_G - V_{TH0}|}{t_{ox}}\right)^{\gamma} t_{stress}^{n}. \quad (3)$$



(a) (b)

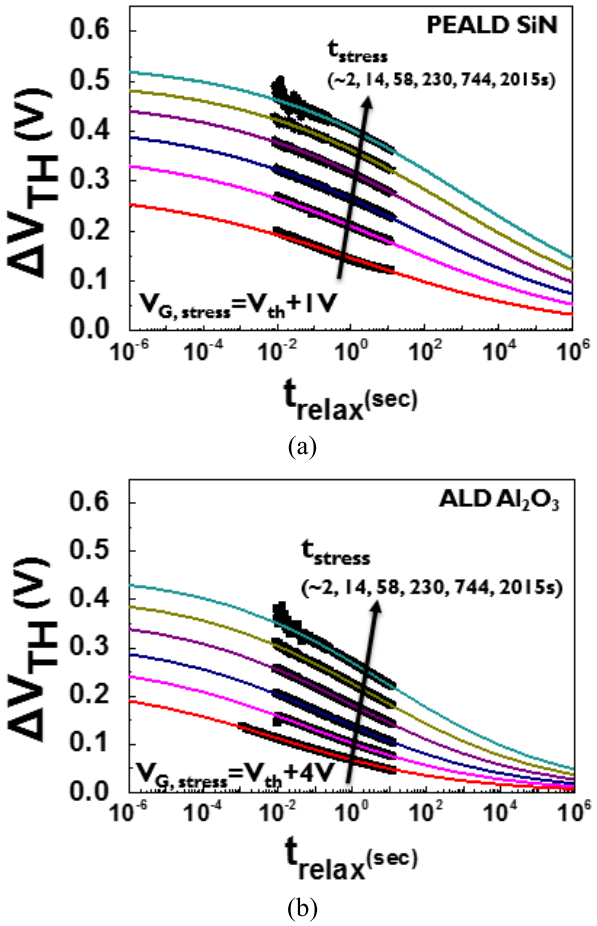
Fig. 9. Arrhenius plots of ΔV_{TH} measured during (a) stress and (b) relaxation on devices with PEALD SiN and ALD Al_2O_3 gate dielectric. The ΔV_{TH} values were extrapolated when the devices were stressed at 1 V of voltage overdrive for 2 s and relaxed for 1 s at different temperatures, i.e., 25 °C, 50 °C, 75 °C, and 100 °C. Similar E_A values are estimated for the emission process when ΔV_{TH} recovery is evaluated from 1 ms to 1 s after stress removal.

Arrhenius plots of the temperature dependence of the measured ΔV_{TH} are shown in Fig. 9 for the different devices. By fitting an exponential trend to the data, one can estimate the apparent ΔV_{TH} activation energy. However, in order to estimate the mean activation energy of the charge capture process, one should consider the time necessary to reach a given ΔV_{TH} (i.e., a given number of charged defects) at different temperatures. Since ΔV_{TH} follows a power law of the stress time with exponent n (3), the activation energy can be obtained by dividing the apparent ΔV_{TH} activation energy for n. The activation energy was estimated to be 0.57/1.02 and 0.67/1.1 eV for the devices with PEALD SiN/ALD Al_2O_3 gate dielectric (time exponent n is 0.10/0.167), respectively. Please note that the electron emission from traps back to the channel could happen during the 1-ms delay (minimum delay) to estimate V_{TH} after the stress removal. Since electron emission is also a thermally activated process, the estimated capture activation energy could be inaccurate. However, the large difference in the value of extracted E_A for the two dielectrics suggests different defect properties, as we will discuss in Section IV.

Another challenge to characterize PBTI is the partial recoverability, once the stress is removed. This is often referred to as relaxation. Such relaxation results in an underestimation of the PBTI degradation with standard delayed measurements. As the eMSM measurement sequence described previously, a set of relaxation curves in the device with PEALD SiN and ALD Al_2O_3 gate-stack were collected, as shown in Fig. 10. The relaxation transients were fitted with the empirical universal relaxation model [22] with the physical assumption of a recoverable (R) and permanent degradation (P) ascribed to different defect types [23], allowing an estimation for the fast ΔV_{th} component from the slowly relaxing (or the so-called permanent) component. While this distinction is only qualitative as it is based on an empirical model, it serves the purpose of further comparing the different PBTI behaviors of the two dielectrics. The ΔV_{TH} recovery can be described as

$$\Delta V_{TH}(t_{stress}, t_{relax}) = R(t_{stress}, t_{relax} = 0) \times r(\xi) + P(t_{stress}) \quad (4)$$

$$r(\xi) = \frac{1}{1 + B\xi^{\beta}} \quad (5)$$



(a) (b)

Fig. 10. Typical set of PBTI relaxation traces measured in the device with (a) PEALD SiN and (b) ALD Al_2O_3 gate dielectric. Note: different stress conditions (gate overdrive and stress time) were chosen in order to yield comparable degradation levels in the two different gate-stacks. The lack of data at short relaxation times (<10 ms) is due to the limited speed of the autoranging feature of the measurement instrument. B and β are 1.06 and 0.15 for the PEALD SiN and 2.72 and 0.18 for the ALD Al_2O_3, respectively.

where t_{stress} is the total stress time, t_{relax} is measured from the end of the last stress phase, $\xi = t_{relax}/t_{stress}$ is the universal relaxation time, and B is a scaling parameter. The functional form of (5) is similar to stretched exponential, which is often used to describe the relaxation of dispersive systems, and β has the attributes of a dispersion parameter. $R(t_{stress}, t_{relax} = 0)$ represents a rough estimation of the full recoverable component extrapolated to $t_{relax} = 0$. Fig. 10 shows the typical set of PBTI relaxation traces, and Fig. 11 shows the recoverable (R) with respect to the different stress times and the permanent degradation (P). The ALD Al_2O_3 shows a smaller recoverable (R) even under a high stress gate voltage and a faster relaxation, as shown in Fig. 10(b). This can also be observed by looking at the ratio between ΔV_{TH} of the ALD Al_2O_3 gate dielectric and the PEALD SiN gate dielectric as a function of the relaxation time (Fig. 12). We can clearly observe that a faster dielectric defect discharge is observed in the device with an Al_2O_3 gate dielectric. This faster relaxation suggests a less favorable defect energy level with respect to the Fermi level in the GaN channel, which induces faster charge emission after stress removal.

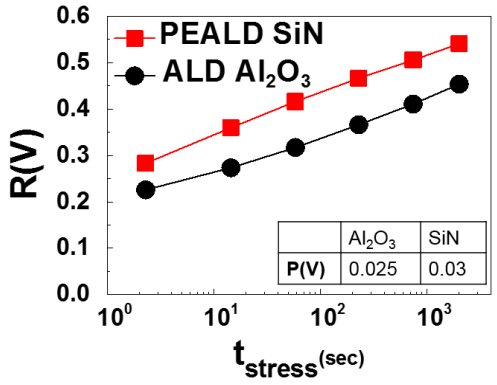


Fig. 11. Recoverable (R) with respect to the different stress times and the permanent degradation (P).

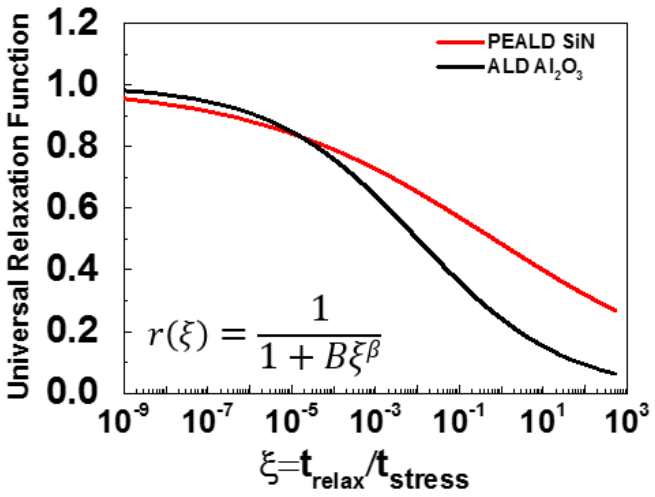


Fig. 12. Transients fitted with the universal relaxation model reveal faster relaxation for the device with Al_2O_3 gate dielectric.

IV. Model

Although Al_2O_3 shows larger D_{it} levels (see Fig. 4), the PBTI-induced V_{TH} shift is smaller compared with SiN. Recent literature shows that the BTI in SiGe [24], Ge [25], [26], and InGaAs [27], [28] devices with high-k gate-stacks is mainly caused by charging/discharging of defects inside the gate dielectric. A dielectric defect band-based model has been used in the literature to successfully describe the BTI in various device technologies. Such model assumes the existence of a normal distribution of dielectric defect levels, and it ascribes BTI V_{TH} shifts to defect filling at varying gate voltages. For simplicity, the model assumes thermodynamic equilibrium, i.e., at each gate voltage, all the defect levels above the channel Fermi level are considered empty, while all the levels below are considered filled. No kinetics is captured by this simplified model, as it would require an accurate description of the lattice relaxation thermal barriers involved in the charging of each individual defect [30]. Therefore, the extracted defect density should be interpreted as the representative of the given stress duration considered (i.e., larger density would be extracted for longer stress data). We note that under the assumption of voltage-independent power-law time exponent, longer stress time would result in a rescaling of the fitted defect densities, but would not modify the defect energy profiles. Furthermore, uniform distribution of defects along the dielectric thickness is assumed, and the applied gate voltage overdrive is assumed to drop solely on the gate dielectric, inducing a constant electric field. The impact of the possible presence of fixed charges is neglected.

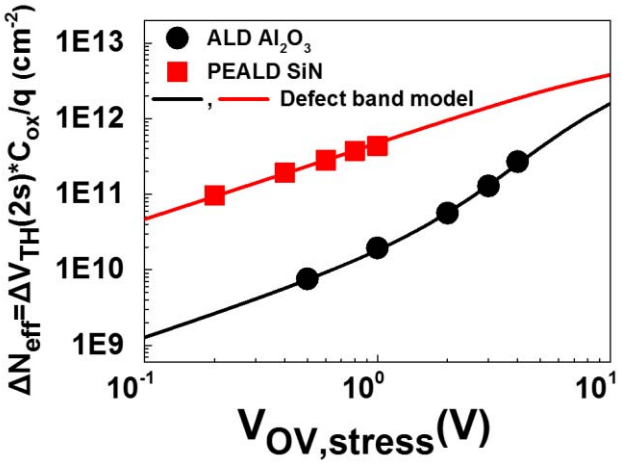


Fig. 13. Experimental data of ΔN_{eff} versus voltage are excellently described by a defect band model calculation, as shown in Fig. 14. The fitting parameters, including D_{ot}, μ_t, and σ_t, are shown in Fig. 14.

Fig. 13 shows the experimental data of voltage dependence of ΔN_{eff} (effective trapped charge density $= \Delta V_{TH} * C_{ox}/q$) against the calculated curves corresponding to the proposed defect band model. Note about the model calculation: the defect bands are modeled as a Gaussian distribution over energy as

$$D_{ot}(E, x) = \frac{D_{ot0}}{\sigma_t \sqrt{2\pi}} \exp\left(-\frac{E - \mu_t(x)}{2\sigma_t^2}\right) \tag{6}$$

where E is the energy within the dielectric bandgap, μ_t and σ_t are the mean and the standard deviations of the Gaussian distributions, and x is the spatial position inside the dielectric layer. Note that μ_t varies across the dielectric thickness to represent the impact of the gate dielectric field, which leverages the trap energy level differently for traps at different gate dielectric depths (see Fig. 14). Charged defects at different spatial positions also contribute differently to the total ΔV_{TH} due to electrostatics. Moreover, an exponential decay term $\exp(-x/x_0)$ is included to account for the reduced tunneling probability of channel electrons toward defects located deeper in the gate dielectric (Wentzel–Kramer–Brillouin approximation for tunneling probability). The characteristic tunneling distance x_0 was fitted as 1.4/2.54 nm for Al_2O_3 and SiN, respectively. Please note that using Gaussian distribution of the defect levels is an assumption for the purpose to simplify the mathematical calculation of the model. Although different energy distributions of the defect might exist in reality, a similar result by shifting up the Fermi level energy in the channel would be obtained independently of the chosen distribution.

As shown in Fig. 14, in order to describe the experimental data, a defect distribution in Al_2O_3 centered ~1.15eV above the GaN conduction band with a relatively narrow

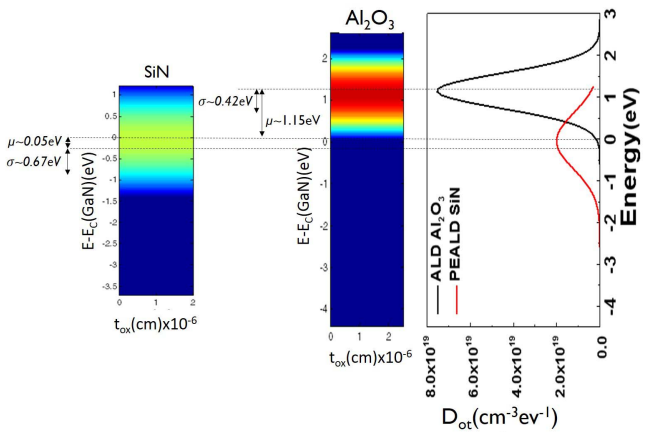


Fig. 14. Defect band models in the device with PEALD SiN gate dielectric and ALD Al_2O_3 gate dielectric (left) and the energy distribution of gate dielectric defects with respect to two different gate dielectrics (right).

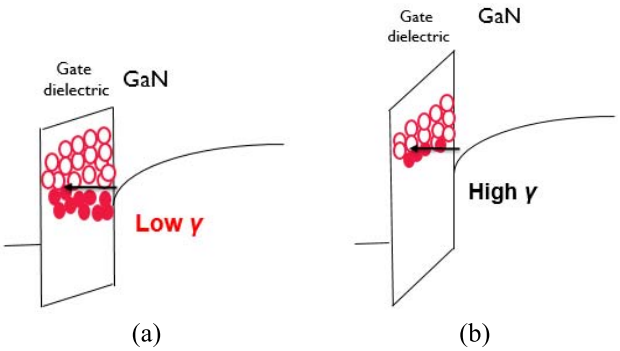


Fig. 15. Illustration of the relation between γ and defect distribution inside the gate dielectric. By comparing the PBTI shift benchmarking in Fig. 8 with the defect band model in Fig. 13. (a) Low γ (similar to the case of PEALD SiN) suggests the existence of a wide distribution of defect level centered around the channel Fermi level. (b) High γ (similar to the case of ALD Al_2O_3) suggests a narrow distribution of defect level far away from the channel Fermi level.

energy spread ($\sigma \sim 0.42$ eV) has to be assumed. In contrast, a significantly wider defect distribution centered around the GaN conduction band has to be assumed for SiN. Interestingly, the total volume density of dielectric defect (D_{ot}) in Al_2O_3 is approximately three times larger than in SiN; however, a large fraction of the defects in Al_2O_3 are not energetically favorable for channel electrons, and therefore, they do not contribute to PBTI shifts at operating condition. On the contrary, the wide defect band in SiN is accessible for channel electrons already at low gate voltages, explaining the large V_{TH} shifts under a low gate bias and the weak voltage acceleration. These results are also qualitatively consistent with the different activation energies estimated (Fig. 9), since the trapping mechanism of the SiN, which has easily accessible dielectric defects, is accelerated less by the temperature, leading to a low activation energy ($E_A = 0.57$ eV) compared with the device with ALD Al_2O_3 ($E_A = 1.02$ eV).

We note that in the framework of the defect band model, the overdrive voltage dependence of ΔV_{TH} (γ in Fig. 8) indicates the accessibility of dielectric defects in the gate dielectric, as shown in Fig. 15. A low γ suggests the existence of a wide distribution of dielectric defects centered around the channel Fermi level, which can be easily accessed at low stress voltage. On the other hand, a high γ suggests a narrow distribution of defect level far away from the channel Fermi level. These physical mechanisms of PBTI in fully recessed-gate GaN MISFETs are also consistent with the understanding of BTI in advanced gate-stacks [31]. Based on all these observations, we conclude that Al_2O_3 gate dielectric is much more promising to improve the PBTI reliability than the SiN gate dielectric.

V. Conclusion

The PBTI reliability of fully recessed-gate GaN MISFETs has been comprehensively investigated. By employing a dedicated set of stress-recovery experiments, i.e., the eMSM technique, we characterized PBTI during both stress and relaxation, highlighting the complex kinetics. The results indicate that: 1) ΔV_{TH} evolution shows a power-law time dependence and 2) PEALD SiN gate dielectric shows a low time exponent n, low voltage dependence of ΔV_{TH} ($\gamma \sim 1$), and low apparent capture activation energy ($E_A = 0.57$ eV), which can be explained by the defect band model we proposed to describe the experimental data. PEALD SiN gate dielectric shows a wide defect band ($\sigma \sim 0.67$ eV) centered 0.05 eV below the conduction band ($E_C - 0.05$ eV) of GaN. In contrast, the defect distribution inside the ALD Al_2O_3 is 1.15 eV away from the conduction band of GaN ($E_C + 1.15$ eV) and shows a narrower energy spread ($\sigma \sim 0.42$ eV). Therefore, the gate dielectric defects inside the PEALD SiN are much more easily accessible under a low gate voltage bias compared with ALD Al_2O_3 gate dielectric, indicating that Al_2O_3 gate dielectric is promising to improve the PBTI reliability. In sum, we have shown that the distribution of defect energy levels inside the gate dielectric can contribute to the PBTI as well, which needs to be considered for further material and process optimization.

References

[1] M. Van Hove *et al.*, "CMOS process-compatible high-power low-leakage AlGaN/GaN MISHEMT on silicon," *IEEE Electron Device Lett.*, vol. 33, no. 5, pp. 667–669, May 2012.

[2] P. Moens *et al.*, "An industrial process for 650 V rated GaN-on-Si power devices using *in-situ* SiN as a gate dielectric," in *Proc. Int. Symp. Power Semiconductor Devices IC's (ISPSD)*, Jun. 2014, pp. 374–377.

[3] S. Yang *et al.*, "High-quality interface in Al_2O_3/GaN/AlGaN/GaN MIS structures with *in situ* pre-gate plasma nitridation," *IEEE Electron Device Lett.*, vol. 34, no. 12, pp. 1497–1499, Dec. 2013.

[4] W. Choi, O. Seok, H. Ryu, H.-Y. Cha, and K.-S. Seo, "High-voltage and low-leakage-current gate recessed normally-off GaN MIS-HEMTs with dual gate insulator employing PEALD-SiN_x/RF-sputtered-HfO_2," *IEEE Electron Device Lett.*, vol. 35, no. 2, pp. 175–177, Feb. 2014.

[5] B. De Jaeger *et al.*, "Au-free CMOS-compatible AlGaN/GaN HEMT processing on 200 mm Si substrates," in *Proc. Int. Symp. Power Semiconductor Devices IC's (ISPSD)*, Jun. 2012, pp. 49–52.

[6] T.-L. Wu *et al.*, "The impact of the gate dielectric quality in developing Au-free D-mode and E-mode recessed gate AlGaN/GaN transistors on a 200 mm Si substrate," in *Proc. Int. Symp. Power Semiconductor Devices IC's (ISPSD)*, May 2015, pp. 225–228.

[7] T.-L. Wu, D. Marcon, M. B. Zahid, M. Van Hove, S. Decoutere, and G. Groeseneken, "Comprehensive investigation of on-state stress on D-mode AlGaN/GaN MIS-HEMTs," in *Proc. IEEE Int. Rel. Phys. Symp. (IRPS)*, Apr. 2013, pp. 3C.5.1–3C.5.7.

[8] P. Lagger, C. Ostermaier, G. Pobegen, and D. Pogany, "Towards understanding the origin of threshold voltage instability of AlGaN/GaN MIS-HEMTs," in *Proc. IEEE Int. Electron Device Meeting (IEDM)*, Dec. 2012, pp. 13.1.1–13.1.4.

[9] P. Lagger, M. Reiner, D. Pogany, and C. Ostermaier, "Comprehensive study of the complex dynamics of forward bias-induced threshold voltage drifts in GaN based MIS-HEMTs by stress/recovery experiments," *IEEE Trans. Electron Devices*, vol. 61, no. 4, pp. 1022–1030, Apr. 2014.
[10] G. P. Lansbergen *et al.*, "Threshold voltage drift (PBTI) in GaN D-MODE MISHEMTs: Characterization of fast trapping components," in *Proc. IEEE Int. Rel. Phys. Symp. (IRPS)*, Jun. 2014, pp. 6C.4.1–6C.4.6.
[11] T.-L. Wu *et al.*, "Correlation of interface states/border traps and threshold voltage shift on AlGaN/GaN metal-insulator-semiconductor high-electron-mobility transistors," *Appl. Phys. Lett.*, vol. 107, no. 9, p. 093507, 2015.
[12] A. Guo and J. A. del Alamo, "Positive-bias temperature instability (PBTI) of GaN MOSFETs," in *Proc. IEEE Int. Rel. Phys. Symp. (IRPS)*, Apr. 2015, pp. 6C.5.1–6C.5.7.
[13] T.-L. Wu *et al.*, "Time dependent dielectric breakdown (TDDB) evaluation of PE-ALD SiN gate dielectrics on AlGaN/GaN recessed gate D-mode MIS-HEMTs and E-mode MIS-FETs," in *Proc. IEEE Int. Rel. Phys. Symp. (IRPS)*, Apr. 2015, pp. 6C.4.1–6C.4.6.
[14] T.-L. Wu *et al.*, "Positive bias temperature instability (PBTI) evaluation in fully recessed gate GaN MIS-FETs," in *Proc. IEEE Int. Rel. Phys. Symp. (IRPS)*, May 2016.
[15] D. Marcon *et al.*, "Direct comparison of GaN-based e-mode architectures (recessed MISHEMT and p-GaN HEMTs) processed on 200 mm GaN-on-Si with Au-free technology," *Proc. SPIE*, vol. 9363, pp. 936311-1–936311-12, Mar. 2015.
[16] S. Liu *et al.*, "Al_2O_3/AlN/GaN MOS-channel-HEMTs with an AlN interfacial layer," *IEEE Electron Device Lett.*, vol. 35, no. 7, pp. 723–725, Jul. 2014.
[17] T.-E. Hsieh *et al.*, "Gate recessed quasi-normally OFF Al_2O_3/AlGaN/GaN MIS-HEMT with low threshold voltage hysteresis using PEALD AlN interfacial passivation layer," *IEEE Electron Device Lett.*, vol. 35, no. 7, pp. 732–734, Jul. 2014.
[18] J.-J. Zhu *et al.*, "Improved interface and transport properties of AlGaN/GaN MIS-HEMTs with PEALD-grown AlN gate dielectric," *IEEE Trans. Electron Devices*, vol. 62, no. 2, pp. 512–518, Feb. 2015.
[19] Y. Hori, Z. Yatabe, and T. Hashizume, "Characterization of interface states in Al_2O_3/AlGaN/GaN structures for improved performance of high-electron-mobility transistors," *J. Appl. Phys.*, vol. 114, no. 24, p. 244503, 2013.
[20] S. Huang, S. Yang, J. Roberts, and K. J. Chen, "Threshold voltage instability in Al_2O_3/GaN/AlGaN/GaN metal–insulator–semiconductor high-electron mobility transistors," *Jpn. J. Appl. Phys.*, vol. 50, no. 11R, p. 110202, 2011.
[21] S. Yang, S. Liu, Y. Li, C. Liu, and K. J. Chen, "AC-capacitance techniques for interface trap analysis in GaN-based buried-channel MIS-HEMTs," *IEEE Trans. Electron Devices*, vol. 62, no. 6, pp. 1870–1878, Jun. 2015.
[22] B. Kaczer *et al.*, "Ubiquitous relaxation in BTI stressing—New evaluation and insights," in *Proc. IEEE Int. Rel. Phys. Symp. (IRPS)*, Apr./May 2008, pp. 20–27.
[23] V. Huard, M. Denais, and C. Parthasarathy, "NBTI degradation: From physical mechanisms to modelling," *Microelectron. Rel.*, vol. 46, no. 1, pp. 1–23, Jan. 2006.
[24] J. Franco *et al.*, "Understanding the suppressed charge trapping in relaxed- and strained-Ge/SiO_2/HfO_2 pMOSFETs and implications for the screening of alternative high-mobility substrate/dielectric CMOS gate stacks," in *Proc. IEEE Int. Electron Device Meeting (IEDM)*, Dec. 2013, pp. 15.2.1–15.2.4.
[25] J. Franco *et al.*, "SiGe channel technology: Superior reliability toward ultrathin EOT devices—Part I: NBTI," *IEEE Trans. Electron Devices*, vol. 60, no. 1, pp. 396–404, Jan. 2013.
[26] J. Ma *et al.*, "AC NBTI of Ge pMOSFETs: Impact of energy alternating defects on lifetime prediction," in *Proc. VLSI*, Jun. 2015, pp. T34–T35.
[27] J. Franco *et al.*, "Suitability of high-*k* gate oxides for III–V devices: A PBTI study in $In_{0.53}Ga_{0.47}As$ devices with Al_2O_3," in *Proc. IEEE Int. Rel. Phys. Symp. (IRPS)*, Jun. 2014, pp. 6A.2.1–6A.2.6.
[28] Z. Ji *et al.*, "An investigation on border traps in III–V MOSFETs with an $In_{0.53}Ga_{0.47}As$ channel," *IEEE Trans. Electron Devices*, vol. 62, no. 11, pp. 3633–3639, Nov. 2015.
[29] M. Cho *et al.*, "Insight into N/PBTI mechanisms in sub-1-nm-EOT devices," *IEEE Trans. Electron Devices*, vol. 59, no. 8, pp. 2042–2048, Aug. 2012.
[30] T. Grasser, "Stochastic charge trapping in oxides: From random telegraph noise to bias temperature instabilities," *Microelectron. Rel.*, vol. 52, no. 1, pp. 39–70, Jan. 2012.
[31] G. Groeseneken *et al.*, "BTI reliability of advanced gate stacks for beyond-silicon devices: Challenges and opportunities," in *Proc. IEEE Int. Electron Device Meeting (IEDM)*, Dec. 2014, pp. 34.4.1–34.4.4.

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